

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

5 Claim 1 (currently amended): An integrated circuit package ~~having central~~  
~~leads~~ comprising:

a substrate having an upper surface, a lower surface and a long slot penetrating from the upper surface to the lower surface, ~~wherein~~ the lower surface ~~is forming~~ ~~formed~~ with a wiring regions arranged at ~~the two sides~~ ~~one side~~ of the long slot, ~~and the wiring regions is formed~~ ~~forming~~ with a plurality of ~~econnected~~  
10 ~~connection points~~, ~~and a the length of the wiring regions are~~ ~~is~~ smaller than a ~~length of the long slot of the substrate~~;

a resistant layer ~~42~~, ~~which~~ is coated on ~~and in contact with~~ the lower surface ~~54~~ of the substrate ~~40~~, and is located between the long slot ~~56~~ ~~and the~~ wiring region ~~58~~, ~~wherein the resistant layer separates the long slot from the~~  
15 ~~wiring region~~, ~~and a length of the resistant layer is substantially equal to the~~  
~~length of the wiring region~~;

a glue layer being coated on the upper surface of the substrate and being located at ~~the~~ ~~a~~ periphery of the long slot;

an integrated circuit having a first surface ~~forming~~ ~~formed~~ with a plurality of  
20 bonding pads and a second surface, the first surface being adhered to the glue layer, ~~then the bonding pads being exposed from the long slot of the substrate~~;

a plurality of wires, each of which is arranged within the long slot of the substrate and ~~is electrically connects~~ ~~econnected~~ the bonding pad of the integrated circuit to the ~~econnected~~ ~~connection~~ point of the substrate; and

25 a first compound layer being filled within the long slot of the substrate for ~~protecting to protect~~ the each wires.

Claim 2 (cancelled).

Claim 3 (currently amended): The integrated circuit package ~~having central~~  
~~leads~~ according to claim 1, wherein the ~~econnected~~ ~~connection~~ points of the lower  
30 surface of the substrate ~~is~~ ~~are~~ formed with a ball grid array (BGA).

Appl. No. 10/705,386  
Amdt. dated November 1, 2006  
Reply to Office action of 07/12/2006

Claim 4 (currently amended): The integrated circuit package having central leads according to claim 1, wherein further comprises ~~comprising~~ a second compound layer, which ~~is covered on~~ covers the upper surface of the substrate.